Analysis and Design of Snubber Networks for dv/dt Suppression in Thyristor Circuits

by J. E. Wojslawowicz

When a triac is used to control an inductive load, voltages with high rates of change (dv/dt) can be generated that can cause a non-gated turn-on of the triac. This false turn-on can occur if the dv/dt exceeds the critical rate of rise of commutation voltage of the triac, or if voltage ringing occurs that exceeds the blocking capability of the triac (V_{DROM}). The false triggering caused by these mechanisms results in a loss of control of power to the load; to assure reliable operation, therefore, it is necessary to provide means to suppress this dv/dt stress as it is commonly called. The simplest method of dv/dt suppression is the use of a series RC network across the main terminals of the triac. The design of this network, commonly called a snubber network, must take into account the peak voltage that can be allowed in the circuit, and the maximum dv/dt stress that the device can withstand. This Note analyzes the RC network design and presents graphs that allow a designer to select a snubber to fulfill his requirements.

Commutating dv/dt And False Turn-On

Fig. 1 shows a control triac in a typical connection with an ac power source and a load. The triac is a regenerative device; once it has been turned on, it continues to conduct until the principal current drops below a value that just supports the regeneration. This current level is called the holding current of the device. If the gate signal is removed before the principal current decreases below the holding current, the device turns off and regains its blocking capability.

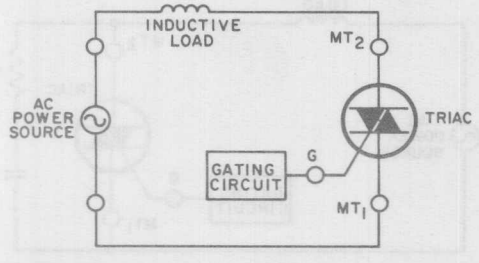

Fig. 1— Series connection of a triac, an inductive load, and an ac power source.

Fig. 2 shows the triac principal voltage and current waveforms when the load is resistive. If the gate signal is removed at time t_o, the device continues to conduct until the current attempts to reverse polarity. The device then undergoes a reverse recovery period, and thereafter must support a main terminal voltage of the reverse polarity that is equal to the source voltage. The rate of reapplication of this off-state voltage for a resistive load and a 120-volt 60-Hz source is typically 0.064 volt per microsecond if the stray inductance due to wiring is minimal. This rate of reapplication generally does not cause turn-on of the device.

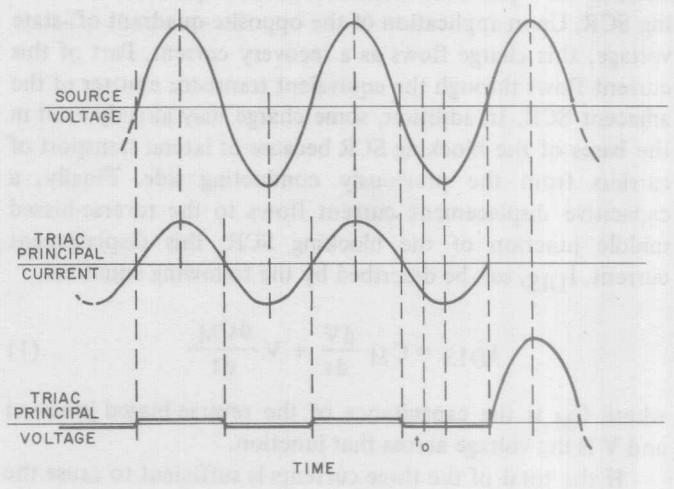

Fig. 2— Principal voltage and current for a triac in operation with a resistive load.

In a circuit with an inductive load the voltage leads the current by some phase angle ϕ as shown in Fig. 3. After the triac turns off it must block the reapplied instantaneous line voltage of the reverse polarity. Because the triac goes from the conducting state to the blocking state in a very short time, this voltage is reapplied very rapidly. The turn-off of the triac causes a rapid decay of current through the inductance, and thus produces an Ldi/dt voltage. This rapidly

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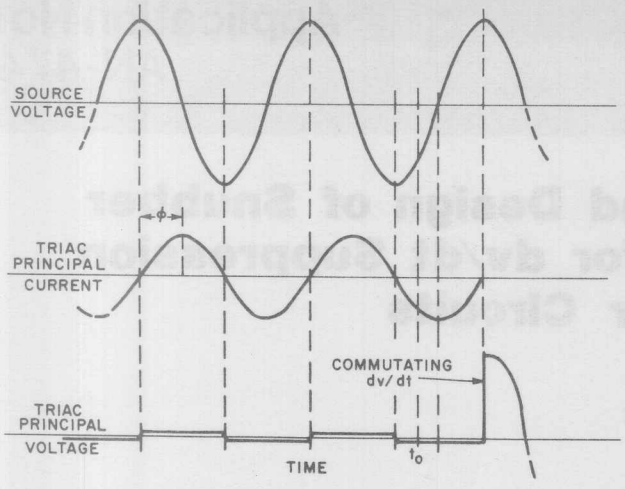

Fig. 3— Principal voltage and current for a triac in operation with an inductive load.

rising off-state voltage stress is impressed across the main terminals of the device and can cause it to turn on. Fig. 4 illustrates this false turn-on.

A triac analog that uses two silicon controlled rectifiers (SCR's) provides a simple understanding of how this dv/dt causes the device to turn on. The inverse parallel SCR analog of the triac is shown in Fig. 5(a), and a two-transistor analog of the SCR is shown in Fig. 5(b). At the end of the half cycle of on-state current conduction, some charge remains in the bases of the equivalent transistors that comprise the conducting SCR. Upon application of the opposite-quadrant off-state voltage, this charge flows as a recovery current. Part of this current flows through the equivalent transistor emitter of the adjacent SCR. In addition, some charge may already exist in the bases of the blocking SCR because of lateral transport of carriers from the previously conducting side. Finally, a capacitive displacement current flows to the reverse-biased middle junction of the blocking SCR; this displacement current, I_{DIS}, can be described by the following equation:

$$I_{DIS} = C_M \frac{dV}{dt} + V \frac{dC_M}{dt} \qquad (1)$$

where C_M is the capacitance of the reverse-biased junction and V is the voltage across that junction.

If the total of the three currents is sufficient to cause the sum of the transistor gains to become unity, the device switches on. The use of the shorted-emitter construction by RCA shunts some of the current away and thus permits a higher dv/dt stress to be placed across the device, but does not eliminate the current completely. The first two current flows are functions of device design and construction, but the displacement current flow can be controlled by use of an RC snubber network that limits the rate of reapplication of off-state voltage.

The snubber network, illustrated in Fig. 6, consists of a resistance R_S and a capacitance C_S placed in series across the main terminals of the device. For some snubber component values and some types of load, excessive ringing can occur in the circuit; this voltage ringing can exceed the blocking capability (V_{DROM}) of the device. Malfunction of the device is then caused by the inability of the triac to block the voltage even though it can withstand the dv/dt stress. An example of voltage ringing is shown in Fig. 7(a). Fig. 7(b) shows the same voltage on an expanded time scale.

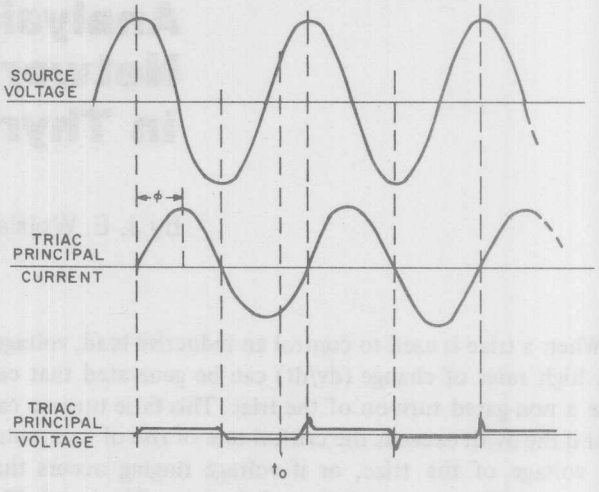

Fig. 4— Principal voltage and current curves showing triac malfunction that results from commutating dv/dt produced by inductive load.

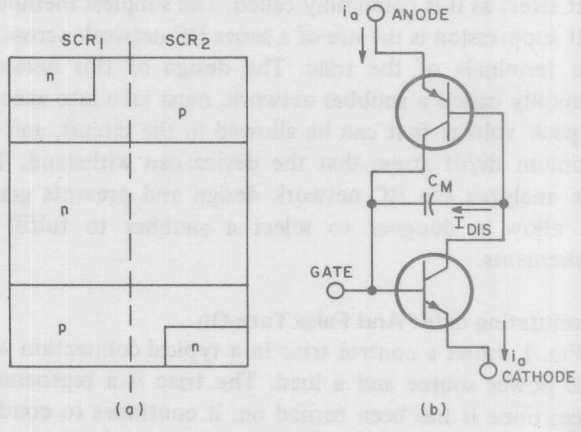

Fig. 5— (a) Two-SCR representation of a triac; (b) two-transistor model of an SCR, with junction capacitance shown.

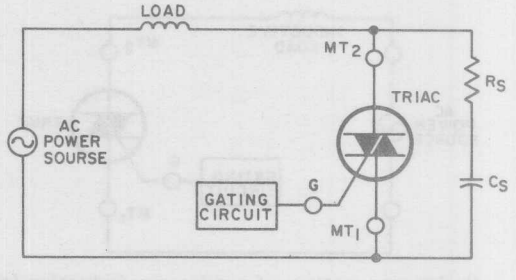

Fig. 6— Triac circuit using a snubber network of R_S and C_S connected across the triac.

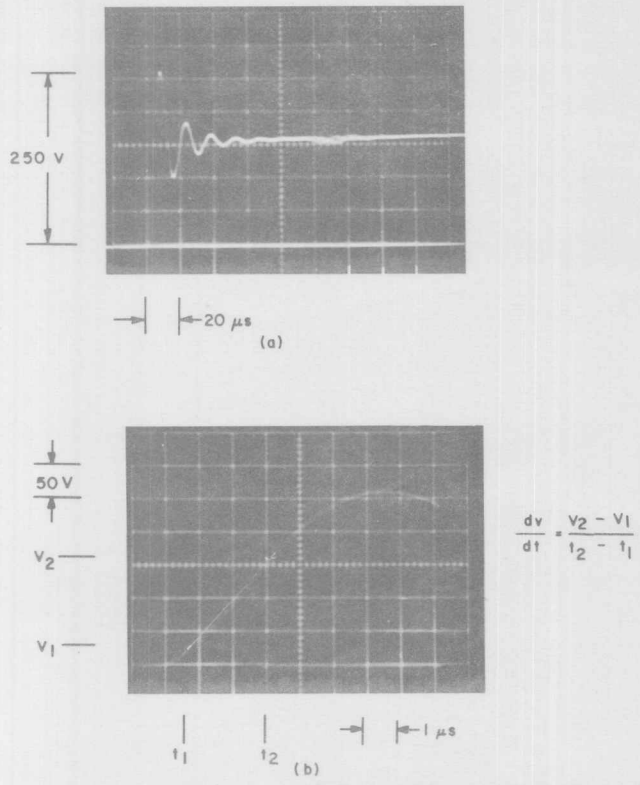

Fig. 7– (a) Ringing, caused by inductive load, in the principal voltage of triac; (b) principal voltage shown on an expanded scale.

Basic Circuit Analysis

The suppression network must be designed to limit the dv/dt stress and to have an acceptable voltage overshoot. Fig. 8 shows an equivalent circuit used for analysis, in which the triac has been replaced by an ideal switch. When the triac is in the blocking or non-conducting state, represented by the open switch, the circuit is a standard RLC series network driven by an ac voltage source. The following differential equation can be obtained by summing the voltage drops around the circuit:

$$(R_L + R_S)\, i(t) + L\frac{di(t)}{dt} + \frac{q_c(t)}{C_S} = V_M \sin(\omega t + \phi) \qquad (2)$$

in which i(t) is the instantaneous current after the switch opens, $q_c(t)$ is the instantaneous charge on the capacitor, V_M is the peak line voltage, and ϕ is the phase angle by which the voltage leads the current prior to opening of the switch. After differentiation and rearrangement, the equation becomes a standard second-order differential equation with constant coefficients. With the imposition of the boundary conditions that i(0)=0 and $q_c(0)$=0, the equation for the charge on the capacitor can be stated for the three circuit conditions as follows:

Condition I[1]: $(R_L + R_S)^2 < 4L/C$

$$q_c(t) = \frac{-|V_M|}{\omega|Z|}\cos(\omega t + \phi + \theta) + |Q_t|\, \epsilon^{-\alpha t} \sin(\beta t + \eta) \qquad (3)$$

Condition II[2]: $(R_L + R_S)^2 = 4L/C$

$$q_c(t) = \frac{-|V_M|}{\omega|Z|}\cos(\omega t + \phi + \theta) + \epsilon^{-\alpha t}\,[(1 + \alpha t)\, q_d + i_d t] \qquad (4)$$

Condition III[3]: $(R_L + R_S)^2 > 4L/C$

$$q_c(t) = \frac{-|V_M|}{\omega|Z|}\cos(\omega t + \phi + \theta) + \frac{\epsilon^{-\alpha t}}{\beta'}[(\alpha q_d + i_d t)\sinh \beta' t + \beta' q_d \cosh \beta' t] \qquad (5)$$

The symbols used in these equations are defined as follows:

$$\phi = \tan^{-1}(\omega L/R_L) \qquad (6)$$

$$\theta = -\tan^{-1}[(\omega L - \frac{1}{\omega C_S})/(R_L + R_S)] \qquad (7)$$

$$\alpha = \frac{R_L + R_S}{2L} \qquad (8)$$

$$\beta' = \sqrt{\left(\frac{R_L + R_S}{2L}\right)^2 - \frac{1}{LC_S}} \qquad (9)$$

$$\beta = \sqrt{\frac{1}{LC_S} - \left(\frac{R_L + R_S}{2L}\right)^2} \qquad (10)$$

$$Z = (R_L + R_S) + j(\omega L - \frac{1}{\omega C_S}) \qquad (11)$$

$$q_d = \frac{|V_M|}{\omega|Z|}\cos(\phi + \theta) + q_c(0) \qquad (12)$$

$$i_d = i(0) - \frac{|V_M|}{|Z|}\sin(\phi + \theta) \qquad (13)$$

$$|Q_t| = \sqrt{\left[\frac{\alpha q_d + i_d}{\beta}\right]^2 + q_d^2} \qquad (14)$$

$$\eta = \tan^{-1}\left(\frac{\beta q_d}{\alpha q_d + i_d}\right) \qquad (15)$$

The voltage across the device is determined by calculating the voltages across the snubber capacitor and resistor from the following fundamental relations:

$$v_{C_S}(t) = \frac{q_c(t)}{C_S} \qquad (16)$$

$$v_{R_S}(t) = R_S\frac{dq_c(t)}{dt} \qquad (17)$$

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No.1CE-402, available on request from RCA Solid State Europe, Customer Technical Data Services, Sunbury-on-Thames, Middlesex, TW16 7HW, England.

RCA/Solid State Europe/Sunbury-on-Thames, Middlesex TW16 7HW, England.

The sum of these two voltages then represents the instantaneous voltage across the triac. The following equations give the instantaneous voltage for the three circuit conditions:

Condition I: $(R_L + R_S)^2 < 4L/C$

$$v(t) = \frac{-|V_M|}{|Z|}\left[\frac{1}{\omega C_S}\cos(\omega t + \phi + \theta) - R_S \sin(\omega t + \phi + \theta)\right] + |Q_t|\epsilon^{-\alpha t}\left[\frac{1}{C_S}\sin(\beta t + \eta) + \frac{R_S}{\sqrt{LC_S}}\sin(\beta t + \eta + \psi)\right] \quad (18)$$

where ψ is defined by the following expression:

$$\psi = \tan^{-1}\left(\frac{\beta}{-\alpha}\right) \quad (19)$$

Condition II: $(R_L + R_S)^2 = 4L/C$

$$v(t) = \frac{-|V_M|}{|Z|}\left[\frac{1}{\omega C_S}\cos(\omega t + \phi + \theta) - R_S \sin(\omega t + \phi + \theta)\right] + \frac{1}{C_S}[(1 + \alpha t)\, q_d + i_d t]\, \epsilon^{-\alpha t} + R_S[(1 - \alpha t)\, i_d - \alpha^2 t q_d]\, \epsilon^{-\alpha t} \quad (20)$$

Condition III: $(R_L + R_S)^2 > 4L/C$

$$v(t) = \frac{-|V_M|}{|Z|}\left[\frac{1}{\omega C_S}\cos(\omega t + \phi + \theta) - R_S \sin(\omega t + \phi + \theta)\right] + \frac{\epsilon^{-\alpha t}}{\beta' C_S}[(\alpha q_d + i_d)\sinh \beta' t + \beta' q_d \cosh \beta' t] + R_S \epsilon^{-\alpha t}\left[\frac{-\alpha i_d - \frac{1}{LC_S} q_d}{\beta'}\sinh \beta' t + i_d \cosh \beta' t\right] \quad (21)$$

A computer is used to calculate the voltage across the snubber because hand calculation is time-consuming. The magnitude and time of occurrence of the peak voltage are found by numerical analysis, and then the values and times of the voltages at 10 per cent and 63 per cent of peak are calculated. These values are used to compute the dv/dt stress as defined by the following equation:

$$dv/dt = \frac{V_2 - V_1}{t_2 - t_1} \quad (22)$$

where V_1 and t_1 are the voltage and time of the 10-per-cent point and V_2 and t_2 are the voltage and time of the 63-per-cent point. This program therefore allows evaluation of various load and snubber combinations in a matter of minutes.

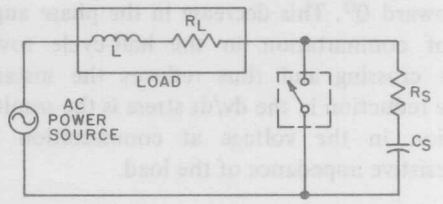

Fig. 8— Equivalent circuit used for analysis.

In general, it is most desirable from a cost standpoint to use a device with the lowest possible V_{DROM} capability. For applications involving the control of a load operating on a 120-volt ac line a device with a V_{DROM} of 200 volts would be desirable; a 400-volt device should be used for operation on a 220-volt line. The use of the lower-voltage device in any application is contingent on the ability of the circuit to limit any possible voltage ringing below the V_{DROM} rating of the device. The snubber can be designed to limit this voltage ringing during the post-commutation period to within this rating. Figs. 9 and 10 show the values of C_S and R_S that limit peak voltage across the triac to specific values. Fig. 9 allows the selection of snubber components that will limit the peak voltage of 200 volts for a zero-power-factor load at the desired dv/dt for an rms line voltage of 120 volts. Fig. 10 shows the components that limit the voltage to 400 volts when the rms line voltage is 220 volts.

Snubber Design Procedure

For use of the graphs, three things must be known: (1) the rms line voltage, (2) the rms load current, and (3) the allowable dv/dt. The following procedure is used to obtain the required snubber components:

(1) Draw a vertical line on the proper voltage graph at the load current.
(2) At the intersection of the vertical line and the dashed line that represents the allowable dv/dt, draw a horizontal line to the right vertical axis. Read the value of R_S from the right vertical axis.
(3) At the intersection of the vertical line and the solid line that represents the allowable dv/dt, draw a horizontal line to the left vertical axis. Read the value of C_S from the left vertical axis.

As an illustration of the above procedure. Fig. 9 is used to find snubber component values that limit the dv/dt stress to 5 volts per microsecond for a 40-ampere rms current in a 120-volt rms line. From Fig. 9, these values are R_s = 340 ohm and C_s = 0.18 microfarad.

As previously stated, these graphs were developed to limit the peak voltage for a zero-power-factor load. For the non-ideal load the graphs are used in the same fashion; a

reduction in the peak voltage following commutation and a slight reduction in the dv/dt stress are the only effects introduced by the non-ideal load. The reduction in the peak voltage excursion is caused by the decrease in instantaneous voltage at the time of commutation. As the power factor increases, the phase angle between the voltage and current decreases toward 0^{o}. This decrease in the phase angle shifts the time of commutation in the half-cycle toward the zero-voltage crossing and thus reduces the instantaneous voltage. The reduction in the dv/dt stress is the result of both the reduction in the voltage at commutation and the increasing resistive impedance of the load.

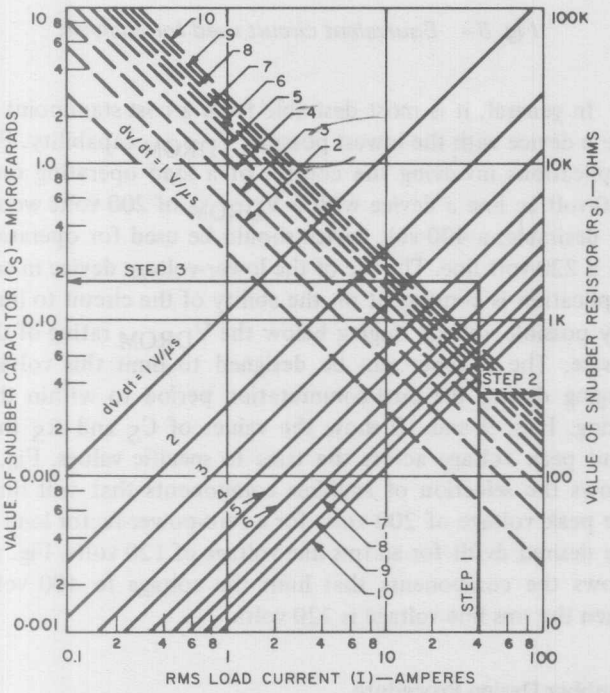

Fig. 9— Design curves for snubber that limits peak voltage to 200 volts for 120-volt ac line and zero power factor.

A numerical example shows how a load that is not purely inductive reduces the peak voltage after commutation. The snubber components for 8 volts per microsecond at an rms current of 22.7 amperes are found from Fig. 9 to be 960 ohms and 0.04 microfarad. If the load is purely inductive, the peak voltage is limited to 200 volts. If the load has the same current rating but a power factor of 0.7, this snubber network limits the peak voltage after commutation to 140 volts. The peak voltage is reduced because the instantaneous line voltage at the time of commutation is only 121 volts. The dv/dt stress is also slightly lower than the 8-volts-per-microsecond value. This example demonstrates that the design graphs of Figs. 9 and 10 can be used for loads having any power factor.

Because the selection of snubber components is dependent on circuit and device characteristics, values obtained may be impractical from a cost or size standpoint. In such a case, a triac with higher dv/dt capability or higher V_{DROM} rating should be used. A higher dv/dt capability allows selection of new snubber components to meet the size and/or cost requirements of the circuit. A higher V_{DROM} rating permits a higher peak voltage excursion that in general will allow selection of a smaller snubber capacitor and smaller resistor.

The circuit analysis described in this Note assumes the effects of the triac to be a minimum. Thus some error is introduced by neglect of the reverse recovery process and the displacement current. The additional current flow tends to increase the instantaneous dv/dt during the first few microseconds following commutation. The over-all effect is to increase slightly the average dv/dt stress across the device. This effect is most noticeable when the snubber capacitance is less than 0.001 microfarad. Selection of a snubber for a lower dv/dt stress limit will generally eliminate this problem.

Because the design of a snubber is contingent on the load, it is almost impossible to simulate and test every possible combination under actual operating conditions. It is advisable to measure the peak amplitude and rate of rise of voltage across the triac after a snubber has been selected.

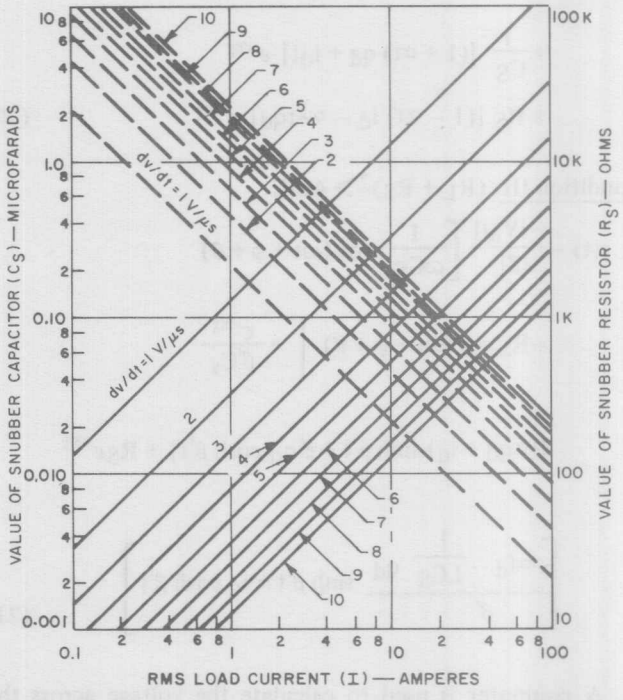

Fig. 10— Design curves for snubber that limits peak voltage to 400 volts for 220-volt ac line and zero power factor.

References

1. Myril B. Reed, Alternating Current Circuit Theory (New York: Harper & Brothers, 1948), pg. 276.
2. Ibid, pg. 284.
3. Ibid, pg. 284.